CLAIMS:

1. An electronic memory component (100 or 100'), comprising at least one memory cell matrix (10), which is embedded in and/or let into at least one doped receiving substrate (20), characterized in that

- the receiving substrate (20) is covered and/or surrounded at least partially and/or on at least one of its surfaces remote from the memory cell matrix (10) by at least one top/protective substrate (30) oppositely doped to the receiving substrate (20) and

- at least one of the substrates (20 or 30), for example the receiving substrate (20) and/or in particular the top/protective substrate (30), is in contact (12a or 12b) or connection (32) with at least one circuit arrangement (24 or 34 respectively) for the detection of voltages or currents caused by charge carriers generated upon light incidence.

2. A memory component as claimed in claim 1, characterized in that the circuit arrangement (24 or 34) takes the form of at least one comparator circuit.

3. A memory component as claimed in claim 1 or 2, characterized in that, if a given limit voltage or a given limit current is exceeded in the circuit arrangement (24 or 34),

-- access to the memory component (100 or 100') may be denied and/or

-- at least one alarm signal may be emitted to at least one controlling C[entral] P[rocessing]U[nit].

4. A memory component as claimed in at least one of claims 1 to 3, characterized in that the top/protective substrate (30) surrounds the receiving substrate (20) in the manner of a well.

5. A memory component as claimed in at least one of claims 1 to 4, characterized in that the top/protective substrate (30) is associated with at least one carrier substrate (40).

6. A memory component as claimed in claim 5, characterized in that the top/protective substrate (30) is buried in the carrier substrate (40).

7. A memory component as claimed in at least one of claims 1 to 6, characterized in that

- the receiving substrate (20) is p-doped,
- the top/protective substrate (30) is n-doped and/or
- the carrier substrate (40) is p-doped.

8. A memory component as claimed in at least one of claims 1 to 7, characterized in that there is associated with the memory cell matrix (10)

- at least one source (12a, 12b) in particular taking the form of a contact,
- at least one bitline (14),
- at least one wordline (16) and
- at least one control gate (18).

9. A memory component as claimed in at least one of claims 1 to 8, characterized in that the memory component (100 or 100') takes the form of an E[rasable] P[rogrammable] R[ead] O[nly] M[emory], an E[lectrical] E[rasable] P[rogrammable] R[ead] O[nly] M[emory] or a Flash memory.

10. Use of an electronic memory component (100 or 100') as claimed in at least one of claims 1 to 9 for in particular continuous detection and/or for in particular permanent sensing of the incidence of light, in particular in the form of at least one light attack, for example on at least one smart card.